ABSTRACT OF THE DISCLOSURE

A display monitor system includes a digital display panel that accepts pixel information in a variety of formats and standards, and adapts itself to send the real-time pixel information directly to the target pixels. An interface controller accepts and conditions NTSC or PAL TV-broadcast formats, and RGB, YUV, DVI, and VGA video formats into pixel information. A timing controller generates a pixel clock, RGB data, and controls for an LCD source driver. This feeds whole rows of pixel information into an LCD array. The timing control also provides line clock and controls to a horizontal-line gate driver associated with the LCD. The interface controller determines odd/even row, and progressive/interlaced timing, and feeds this control information to the horizontal-line gate driver. In an alternative embodiment, a transducer is associated with each pixel in the LCD array, and its information can be read out. The LCD array is therefore addressed as if it was a random access memory (RAM).